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| 08/984,563 | 12/03/1997 | JEFFREY S. MAILLOUX | 95-0653.03 | 2304 |

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| EXAMINER | |
|---|---|
| KIM, HONG CHONG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | 33 |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 08/984,563 | Applicant(s) MAILLOUX ET AL. | |
|---|---|---|---|
| | Examiner Hong C Kim | Art Unit 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *36-39,59-69 and 75-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36-39,59-69 and 75-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

**Detailed Action**

1. Claims 36-39, 59-69 and 75-83 are presented for examination. This office action is in response to the appeal brief filed on 5/16/03.

2. In view of the appeal brief filed on 5/16/03, PROSECUTION IS HEREBY REOPENED. It appears that claims 65-67 are contained allowable subject matter. Claims 65-67 would be allowable if overcame double patenting rejection. However, claims 36-39, 59-64, 68-69 and 75-83 are rejected again with new arguments, specifically claim 68 has been rejected under 35 USC 102(e) instead of 103(a). The examiner apologies for any inconveniences.
A ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

3. It is noted that this application appears to claim subject matter disclosed in the co-pending

section or related section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending or related applications to avoid possible double patenting (i.e U.S Pat. No 5966724).

## *DOUBLE-PATENTING*

4. The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5 Claims 65-67 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 51, 59, 63, 64, and 67 of copending Application No. 08/984,561. Although the conflicting claims are not identical, they are not patentably distinct from each other because both sets of claims are related to a method of accessing a storage device, comprising: maintaining a first enabling signal in an active state, selecting burst and pipelined mode, receiving an initial external address, selecting read and write operation, cycling a second enabling signal, generating an internal address, switching the mode of operation to a pipeline mode. Both sets of claims recited similar inventive concept of accessing a memory in burst and pipelined mode except: Claims 65-67 of the present invention comprises less element than as claimed in the Application No. 08/984,561. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to delete additional limitation of maintaining a first enabling signal in an active state of the copending application to arrive invention of the present application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(b) the invention was patented or described in a printed publication in this or a foreign

country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 36-39, 59-64, 68-69, and 75-83 are rejected under 35 USC 102(e) as being anticipated by *Manning*, U.S. Patent 5,610,864.

As to claim 59, *Manning* discloses a method of accessing a memory (Fig. 1 ), comprising: receiving an external row address (Fig. 1 and Fig. 2, ADDR, ROW); choosing whether the memory is in burst (col. 6 lines 14-26 and col. 7 lines 43-54) or a pipelined mode of operation (col. 5 lines 43-50) ("The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture

is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); and executing a read or write operation (Fig. 2, /WE).

As to claim 60, *Manning* further discloses switching between a burst mode (col. 6 lines 14-26 & col. 7 lines 43-54 and Fig. 1) and a pipeline mode (col. 5 lines 43-50).

As to claims 61, *Manning* further discloses switching between a read and a write operations (Fig. 2 /WE).

As to claim 62, *Manning* further discloses the operations are performed in a different order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+).

As to claims 36, 75, and 80, *Manning* discloses the invention as claimed. *Manning* discloses a method for accessing an asynchronously access memory (Fig. 1 and EDO constitutes asynchrous memory, col. 6 lines 14-16), comprising the steps of: receiving an external row address to the asynchronously accessible dynamic random access memory accessible storage device (Fig. 1 and

Fig. 2, ADDR, ROW); selecting or switching between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50) ("The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); and obtaining a first external column address (Fig. 1 and Fig. 2, ADDR, COLm).

As to claims 37, 76, and 81, *Manning* further discloses the step of obtaining a second external column address subsequent to the first external column address for operation in the pipeline mode (col. 5 lines 43-45). "The current invention include a pipelined architecture where memory accesses are performed sequentially --- In a pipelined architecture the overall throughput of the memory approaches one access per cycle" (col. 5 lines 43-49 in Manning) reads on this limitation since the second address should be provided subsequent to the first external address in a pipelined mode operation. In other words, accessing a non burst memory such as a standard EDO memory including a pipelined architecture, a new external address should be provided to an input address terminal every memory access cycle in order to take an advantage of the pipelined architecture since the pipelined architecture effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe.

As to claim 38, *Manning* further discloses generating internal address (col. 5 lines 51-62 and col. 8 line 67).

As to claims 39, 77, and 82, *Manning* further discloses selecting path way (Fig. 1 Ref. 40 and col. 3 lines 20-22, col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+).

As to claims 78 and 83, *Manning* further discloses switching between the pipelined mode of operation (col. 5 lines 43-50) and the burst (col. 6 lines 14-26 and col. 7 lines 43-54) and

generating internal address (col. 5 lines 51-62 and col. 8 line 67).

As to claim 79, *Manning* further discloses selecting at least one address pathway based on subsequently switching to the burst mode of operation (Fig. 1 Refs. 40 &. 26, controlling the column address counter/latch between burst and pipelined modes reads on this limitation, because during the burst operation, the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies, col. 3 lines 19-21 and col. 5 lines 50-57, however, during the pipelined operation, each column address is provided one access per cycle, col. 5 line 43-50. In other words, during the burst mode, an internal counter/latch path is selected however, during the pipelined mode, an external counter/latch path is selected, see also col. 6 lines 26-34).

As to claim 63, *Manning* discloses a method of accessing a memory (Fig. 1 ), comprising: receiving an external row address (Fig. 1 and Fig. 2, ADDR, ROW); selecting a burst mode operation (col. 6 lines 14-26 and col. 7 lines 43-54) or a pipelined mode of operation (col. 5 lines 43-50) ("The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode. Also it is well

known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); executing a read or write operation (Fig. 2, /WE); and selecting an external address only path, obtaining external address for both read and write operation if the pipelined mode operation is selected and selecting an initial buffered external address data path, obtaining an initial external column address, obtaining information, generating internal column address then obtaining further information from the memory until all desired internal column addresses are used for both read and write operation if the burst mode operation is selected (Fig. 1 Refs. 40 &. 26, controlling the column address counter/latch between burst and pipelined modes reads on this limitation, because during the burst operation, the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies, col. 3 lines 19-21 and col. 5 lines 50-57, however,

during the pipelined operation, each column address is provided one access per cycle, col. 5 line 43-50. In other words, during the burst mode, an internal counter/latch path is selected however, during the pipelined mode, an external counter/latch path is selected, see also col. 6 lines 26-34).

As to claim 64, *Manning* further discloses the operations are performed in a different order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col. 6 lines 14+).

As to claim 68, *Manning* discloses a method for data transfer direction selection in a memory (Fig. 1 ), comprising: selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); selecting a burst mode operation (col. 6 lines 14-26 and col. 7 lines 43-54) or a pipelined mode of operation (col. 5 lines 43-50) ("The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by

overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.); and selecting an external address only path, obtaining external address when the pipelined mode operation is selected and selecting an initial buffered external address data path, obtaining an initial external column address, accessing the memory, and generating internal column address when the burst mode operation is selected (Fig. 1 Refs. 40 &. 26, controlling the column address counter/latch between burst and pipelined modes reads on this limitation, because during the burst operation, the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies, col. 3 lines 19-21 and col. 5 lines 50-57, however, during the pipelined operation, each column address is provided one access per cycle, col. 5 line 43-50. In other words, during the burst mode, an internal counter/latch path is selected however, during the pipelined mode, an external counter/latch path is selected, see also col. 6 lines 26-34).

As to claim 69, *Manning* discloses a storage device (Fig. 1 ), comprising: mode circuitry configured select between a burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode (col. 5 lines 43-50) ("The current invention include a pipelined architecture where memory

accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.); selection circuitry for selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); executing a read or write operation (Fig. 2, /WE); and an external column address data path (Fig. 1 Refs. 40 &. 26, controlling the column address counter/latch between burst and pipelined modes reads on this limitation, because during the burst operation, the address is incremented internal to the device eliminating the need for external address lines to switch at high frequencies, col. 3 lines 19-21 and col. 5 lines 50-57, however, during the pipelined

operation, each column address is provided one access per cycle, col. 5 line 43-50. In other words, during the burst mode, an internal counter/latch path is selected however, during the pipelined mode, an external counter/latch path is selected, see also col. 6 lines 26-34); an internal column address generation module (Fig. 1 Ref. 26 col. 3 lines 19-21 and col. 5 lines 50-57); and pipeline (col. 5 lines 41-50)/burst circuitry (col. 6 lines 14-26 & col. 7 lines 43-54 and Fig. 1 Ref. 38 & 40) .

***Response to Amendment***

8. Applicant's arguments filed on 5/19/2003 have been fully considered but they are not persuasive.

In response to applicant's argument at the center of pages 5-7 in the Appeal Brief that the cited references do not disclose "selecting or switching between a burst mode and a pipelined mode" has been fully considered but it is not persuasive.

Manning (864) discloses selecting or switching between a burst mode and a pipelined mode. "The current invention include a pipelined architecture where memory accesses are performed sequentially" (col. 5 lines 43-49 in Manning) and "switching between burst EDO mode and standard EDO mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation. In other words, in order to work in a standard EDO memory including a pipelined architecture, one has to select a pipelined mode if one is in a burst mode. Also it is well known in the memory art that the pipelined memory architecture provides speed advantages by enabling

more than one memory read, memory write, memory address input, memory data input or memory data output to be processed simultaneously. In other words, the pipelined architecture advantage in a memory effectively hides memory wait state, specifically this is accomplished by overlapping memory operations using a pipe. Another advantage that the pipelined memory architecture has over the parallel read and write architecture is a reduction in required circuitry. In particular, the parallel architecture requires two sample-and-hold circuits (one in each buffer) per read or write circuit. The pipelined architecture requires only a single sample-and-hold circuit per read or write circuit. Thus, the pipelined architecture can reduce circuit cost by decreasing the required integrated circuit area.

Therefore broadly written claims are disclosed by the references cited.

### *Allowable Subject Matter*

9. It appears that claims 65-67 are contained allowable subject matter. Claims 65-67 would be allowable if overcame double patenting rejection.

### *Conclusion*

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time

policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

13. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matt Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

15. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

**or faxed to TC-2100:**
After-Final (703) 746-7238
Official (703) 746-7239 (for formal communications intended for entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
August 9, 2003